# A High Power On-Wafer Pulsed Active Load Pull System

Dennis D. Poulin, *Member, IEEE*, John R. Mahon, and Jean-Pierre Lanteri

*Abstract*—**This paper describes a unique on-wafer load pull system that is capable of measuring load pull contours on true high power and large periphery devices. Measurements are made under low duty cycle pulsed dc and RF conditions to minimize the effects of heating due to power dissipation in the on-wafer environment. With the current implementation of the load pull system, any load impedance on the Smith chart can be presented to the output of four Watt devices. The system is fully error corrected for reflection coefficient, transmission coefficient, input power incident, input power delivered, and output power delivered. The system is capable of automatic control and measurement by means of a HP 9000 series workstation. Data taken on *C* band MMIC power amplifiers and 2 mm GaAs FET's are presented.**

## Introduction

LOAD PULL SYSTEMS are used to obtain design information on large signal, high power devices or to robustly verify the validity of nonlinear models for high power devices. The most desirable form of load pull information is data taken on devices that are still in wafer form using a microwave probe station. Unfortunately, previous approaches to load pull systems were ill suited for the on-wafer environment due to a variety of reasons. The passive load pull systems can not overcome the significant loss associated with microwave probe stations. This results in an inadequate range of load impedances that can be presented. The active load pull systems are not limited by the probe system loss. However, these systems are all based on cw measurements using a standard cw vector analyzer. This cw operation is unacceptable for the on-wafer environment for devices that have gate widths more than 500 $\mu$M due to the high dc power dissipation and the poor heat sinking in wafer form. The load pull system presented here overcomes these limitations and uses a more complete error correction for impedance parameter, transmission parameter and power measurements. The main contributions demonstrated in this paper include:

1) An expandable active load pull approach that currently is capable of presenting any arbitrary load impedance at the device pads for devices that can deliver up to 4 W of power output in an on-wafer environment.
2) A pulsed dc and pulsed RF measurement environment that prevents the wafer form device from overheating due to power dissipation.
3) A programmable electronic approach to the adjustment of phase and amplitude for the "reflected" component of the effective load impedance.
4) A robust error correction scheme that utilizes vector error correction for input impedance, load impedance, insertion gain, power delivered to the input, power incident to the input and power delivered to the load.

This paper discusses the configuration of the on-wafer load pull system, the system considerations, the error correction approach, the presentation of data taken on the system and a discussion of future enhancements.

## System Description

The on-wafer pulsed active load pull is based on a variation of the Takayama active load pull system [2]. A simplified block diagram for the system is shown in Fig. 1. A unique aspect of the load pull system is the use of separate 10 W TWTA's for the input and the output of the system. The two TWTA approach allows for adequate power to be made available for the output side of the system to obtain any effective load impedance on the Smith chart presented at the output side probe tip independent of the power requirements for the input side of the system. The 10 W output side TWTA was experimentally verified to be sufficient to be able to provide arbitrary tuning to on-wafer devices that delivered up to 4 W of delivered power into their optimum impedance.

The second 10 W TWTA is used to provide the input drive for the system. This TWTA was experimentally verified to be sufficient to provide drive levels of up to +25 dBm delivered to the input of a 2 mm wide device in an untuned, 50 Ω environment. A broad band, real impedance is maintained on the input side of the system to terminate any harmonics emanating from the input of the device. In this system, any harmonics from the input of the device will be terminated in approximately 50 Ω by the isolator after the input TWTA. Even order harmonics are generated at the input of the device when the gate to source junction is forced into forward conduction by large input RF drive levels. The onset of this harmonic gener-

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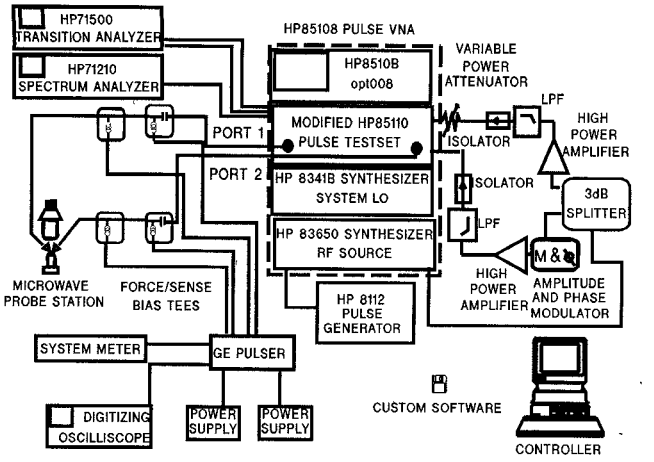



Fig. 1. Simplified block diagram for pulsed active on-wafer load-pull system. The foundation of the system is a HP 85108 Pulsed Vector Network Analyzer.

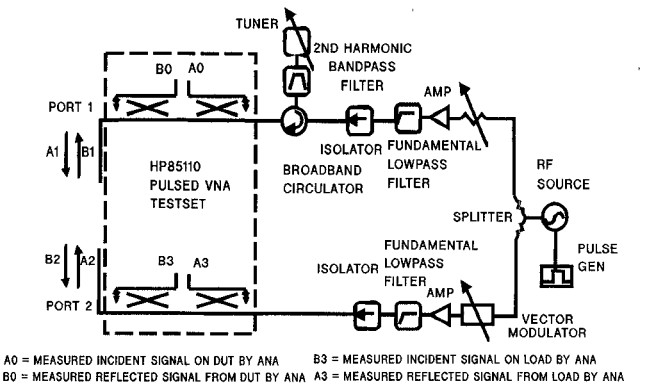



Fig. 2. Simplified block diagram of system used to investigate the impact of second harmonic termination at the input of the DUT under power saturated conditions.

ation can be monitored by observing the amount of dc gate current. The distortion to the input waveforms due to this harmonic generation has been experimentally measured and reported in earlier work by several researchers including F. Siechi, formerly of RCA Sarnoff Labs. Any attempt at "helping out" the input TWTA by inserting an input tuner in the system can result in non repeatable results under large signal conditions due to the highly reflective and arbitrary nature of the harmonic termination of the input tuner as a function of tuner setting. This assertion had been verified in a qualitative fashion in some earlier work using the measurement system block diagram shown in Fig. 2. The frequency selective tuner at the input of this system will only change the amount of second harmonic that will be re-reflected back towards the input of the device. As the tuning on the second harmonic is changed under conditions of fundamental compression, the dc gate current is observed to change which can consequently slightly shift the dc operating point. These shifts can lead to repeatability problems in a load pull system with an input tuner unless the input tuner is constrained to repeat its tuning point. This issue goes away in a load pull system that maintains 50 Ω on the input side.

The heart of the measurement system is a HP 85108 pulsed vector network analyzer. This system includes a HP 8510B opt 008 vector receiver with an IF bandwidth of 2.5 MHz to obtain maximum sensitivity under pulse conditions and a HP 85110 high power mixer based test set that has expansion links that are used to install the additional hardware needed for the active load pull. In addition, the test set has been modified to incorporate a HP 71500 microwave transition analyzer. The modification entails switches that were placed in the coupled arms of the directional couplers in the test set such that either the HP 8510B or the HP 71500 can be used as the vector receiver. The use of the transition analyzer is discussed in the section on future work. All the vector error correction for the ratio measurement is done utilizing the internal error correction capabilities of the HP8510B vector network analyzer.

In addition to the vector ratio measurements for the input impedance, load impedance and insertion gain, the HP8510B receiver is used to measure the absolute power at the input and output of the device under pulsed conditions. Each unratioed parameter, USER1, USER2, USER3, and USER4, has been characterized for power linearity and correction factor to obtain the error corrected values that correspond to power incident on and reflected from the device under test and the power incident on and reflected from the load. When done in this fashion, the error coefficients for the power measurements are simple extensions of the normal 12 term error coefficients obtained for the ratio measurements.

Load pull contours can be generated for either conditions of constant incident input power or constant delivered input power. Delivered power is defined as the difference between the power incident and the power reflected in Watts. Incident power to the device under test has to be vector error corrected to account for the limited raw source match of the input side of the test system and the limited S12 of the device under test as a function of load impedance under large signal conditions. Delivered power to the input is usually used for discrete devices to simulate the same conditions as conjugate match. Error corrected incident power to the input is usually used for amplifier MMIC's to simulate a 50 Ω environment. All the error correction for power is done remotely using computer control with an HP 9000 series workstation.

The high current pulsed dc for the device drain is produced by means of a pulse modulator built by GE for a phase 3 MMIC project [7]. The pulsed dc is applied to the test system by means of a pair of modified bias tees. Both a "force" tee and a "sense" tee are used to account for Ohmic drops in the test system. The inductor feeds in the bias tees have been modified to decrease their inductance and increase their current handling capability. These special bias tees are available from Hewlett Packard as a special option on the standard bias tees. Pulsed currents of up to 10 A and voltages of up to 20 V can be supplied to the system as long as a low duty cycle and moderate pulse widths are used.

The selection of pulse width and duty cycle must meet certain criteria. The "off" time of the pulse must be long enough such that the on-wafer device has time to return to ambient temperature. For devices that dissipate a dc power of 15 W, it was experimentally determined that 270 $\mu$S of "off" time was sufficient to return the on-wafer device to ambient temperature from its operating temperature. It was also experimentally determined that this type of device could survive a dc pulse up to 400 $\mu$S wide without damage. The narrowest dc pulse that could be produced and measured by the GE pulser was 1 $\mu$S wide. The network analyzer can sample the data anywhere in the pulse with a 200 nS resolution. The system is synchronized with a pair of pulse generators. The RF output power droop versus sampling point in the pulse was measured for a 4 W HPA dissipating 15 W of dc power. The droop was less than .1 dB between a sampling point of 15 $\mu$S versus a sampling point of 200 nS. After several iterations, a dc pulse that has a pulse width of 30 $\mu$S, a duty cycle of 10%, and a measurement sampling point at 15 $\mu$S into the pulse was used as a standard measurement configuration. This combination yielded repeatable results on-wafer and gave good agreement with fixtured data and data taken previously with smaller pulse widths and sampling points.

In an active load pull system, the load impedance is synthesized by taking a portion of the input drive, amplitude and phase shifting the signal, amplifying it and sending it to the output of the device under test. This signal takes the place of the wave "reflected from the load" under passive conditions. The effective load impedance generated is measured in real time by the vector error corrected reflectometer on the output side of the load pull system. The phase and amplitude adjustment is traditionally done using electromechanical line stretchers and variable attenuators. These "tuning" elements are slow to automate and are subject to mechanical wear. Electromechanical devices were initially used to verify operation of the load pull system. The final active load pull presented here utilizes a complete electronic approach to the tuning. The phase and amplitude adjustment is performed by an I–Q vector modulator that is inserted at the input of the "load" TWTA. Since it is at the input of the TWTA, it does not have to withstand high power levels and any harmonics generated by the modulator are filtered by the low pass filter after the TWTA. The TWTA is operated in a more or less linear fashion and any amplitude or phase change at the input will be replicated on the output. The effective load impedance is measured in real time by the system and it is not necessary to "predict" the exact amplitude and phase change. The vector modulator is continuously variable over one quadrant and this variable quadrant can be switched to any of the three remaining quadrants. Block diagrams of two alternative approaches to the continuously variable section are shown in Fig. 3. The phase and amplitude is changed in the modulator by means of dc levels applied to the I and Q inputs from two 10 bit bipolar DAC's. This type of modulator has greater

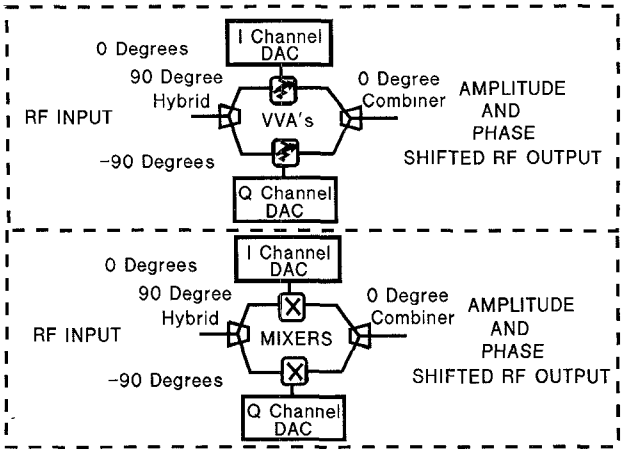



Fig. 3. Block diagrams for Voltage Variable Attenuator based and Mixer based electronically controlled continuously variable 90 Degree Vector Modulators. Range is 0–90 degrees in phase and 0–40 dB change in amplitude.

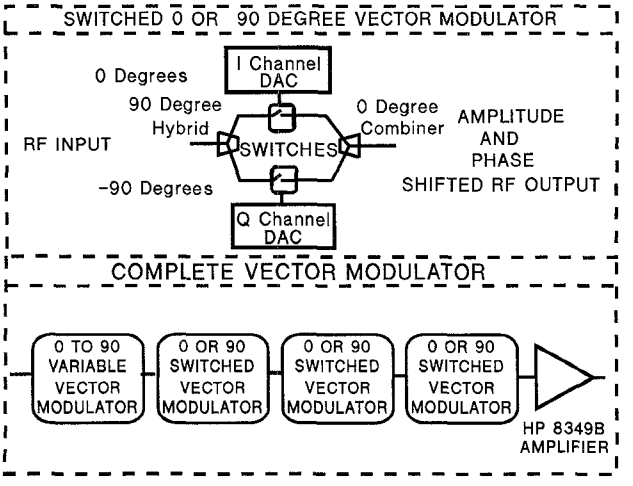



Fig. 4. Block diagram for Switched Vector Modulator that is used to obtain either 0 or 90 degrees of phase shift. Block diagram of complete Vector Modulator. Complete modulator achieves 0–360 degrees in phase and a change in amplitude between 0 and 40 dB.

than 40 dB of amplitude range and a 90 degree phase range. Either voltage variable attenuators or mixers can be used to control the amplitudes in the SINE and COSINE legs of the vector modulator. Both approaches were breadboarded and provided adequate performance. The VVA approach was chosen for the final modulator since it was lower cost and less prone to damage and distortion. The quadrant switching sections are shown in Fig. 4 as well as the complete modulator. The complete modulator also incorporated a medium power amplifier to compensate for the insertion loss of the modulator.

## Error Correction

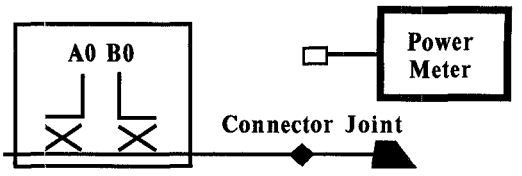
The systematic errors in the load pull system are all linear and time invariant. Upon inspection of the signal flow graphs for both a "standard $S$ parameter" configuration and the active load pull configuration for the HP85108 pulse vector network analyzer, it is observed that the sources of the error coefficients are identical. The

only differences occur when the calculations for "error corrected" data are performed. Therefore, the error coefficients for the system are extracted using the system in a "*S* parameter" configuration with a conventional on-wafer calibration (SOLT, TRL, LRM). Because of the nature of the modifications made to the system to use it as an active load pull, the network analyzer must be calibrated with the assistance of a computer. First, the raw data for each calibration standard is measured and stored to disc. This step is necessary because the active load on the output of the system needs to be changed between the forward and reverse measurements. The "raw" standard data is then triggered into the HP 8510B using the SIMS command to perform a "simulated" calibration. The error coefficients will then be available for the various error corrections.

In an active load pull setup it is awkward and slow to continuously call up the individual parameters, (USER1, USER2, USER3, USER4), in order to measure power at the same time as the measurement of the desired ratios, (S11, S21, 1/S22). Since all of the ratio measurements are "forward" measurements, it is convenient to base all of the power measurements on just the (USER1) parameter. This is done by a two tier calibration procedure and a clever use of the resultant error coefficients and the corrected ratio measurements. The first "tier" in the calibration procedure is at a convenient coaxial interface point that just precedes the input probe. A one port coaxial calibration is performed at this interface as well as a measurement of absolute power with a power meter and the (USER1) channel of the HP8510B. This establishes a "known" reference plane for the initial power correction and the corresponding effective source match at the reference point. The input microwave probe is reconnected to the reference point. The second tier is accomplished by performing a standard 10 term (isolation omitted) error correction at the probe tips. The error coefficients from both the one port calibration and the two port calibration are then extracted by the computer and used to translate the power measurement "sense" port from the coaxial reference plane to the input probe tip. Fig. 5 summarizes this procedure.

Some notation conventions were adopted to assist in the error correction flow graphs. The measured incident and reflected signals on the input side are (a0) and (b0) which correspond to (USER1) and (USER2) on the network analyzer. The actual incident and reflected signals at the DUT input are (a1) (incident) and (b1) (reflected). The actual (incident and reflected signals at the actual load are (b2) (incident) and (a2) (reflected). Note that the load notation is "inverted" from normal convention. The measured incident and reflected signals on the "load" side are (b3) and (a3) which correspond to (USER3) and (USER4) on the network analyzer. The error coefficients (e00) and (e33) correspond to "directivity" terms, (e11) and (e22) correspond to "system match" terms, and (e10), (e01), (e32) and (e23) correspond to "tracking" terms.

Fig. 6 shows some of the flow graphs that were used in




A0 = INCIDENT SIGNAL MEASURED ON PORT 1 BY HP8510B ANA (USER 1)
B0 = REFLECT SIGNAL MEASURED ON PORT 1 BY HP8510B ANA (USER 2)

1.) VERIFY POWER LINEARITY OF A0 (USER 1) USING POWER METER.
2.) PERFORM 1 PORT CAL AT CONNECTOR JOINT.
3.) DETERMINE CAL OFFSET BETWEEN A0 AND ABSOLUTE POWER AT CONNECTOR JOINT USING THE POWER METER.
4.) PERFORM A FULL 2 PORT CAL AT THE WAFER PROBE TIPS.
5.) EXTRACT CAL COEFFICIENTS FROM BOTH CALS AND DE-EMBED PATH FROM A0 TO PROBE TIP.
6.) USE EXTRACTED CAL COEFFICIENTS TO CALCULATE ERROR CORRECTED INPUT POWER INCIDENT AND DELIVERED TO DUT.

Fig. 5. Calibration procedure used to calibrate the USER 1 channel of the HP8510B VNA to measure error corrected incident or delivered input power under pulsed conditions.

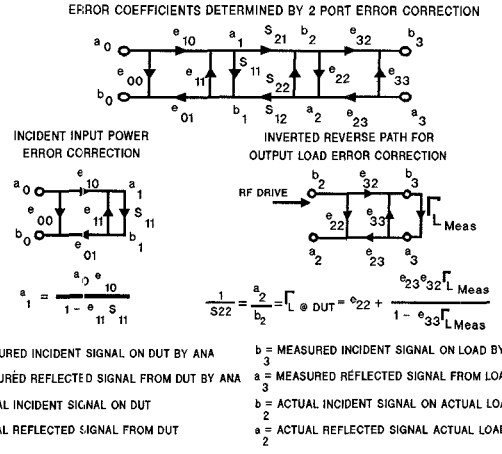



Fig. 6. Flow graphs used for error correction of power in, power out, gain, input reflection coefficient and load reflection coefficient. Error terms are traditional VNA error terms for directivity, source match, and tracking.

the error correction. The input reflection coefficient is corrected in the traditional fashion. The load reflection coefficient error correction follows the same form as a traditional error correction except that the quantity that is corrected is (1/S22). The corrections for the power measurements are similar to those proposed by Tucker and Bradley [3] except that the error corrections for power incident to the device under test are also calculated. By proper input into the error correction matrix in the HP8510B, all the ratioed measurements can be displayed fully error corrected. All the power measurements and corrections are done in the controlling computer. The power measurements in the system are based on readings taken from the (USER1) "raw" data on the HP8510B combined with the error corrected *S* parameters of the device under test and the previously determined system vector error correction coefficients. The power incident on the device under test is error corrected to account for the limited source match of the input side of the system. The power incident on the load will simply be this error corrected power incident on the device under test multiplied by the square of the error corrected value of S21 for the device under test. The power delivered to the load is de-

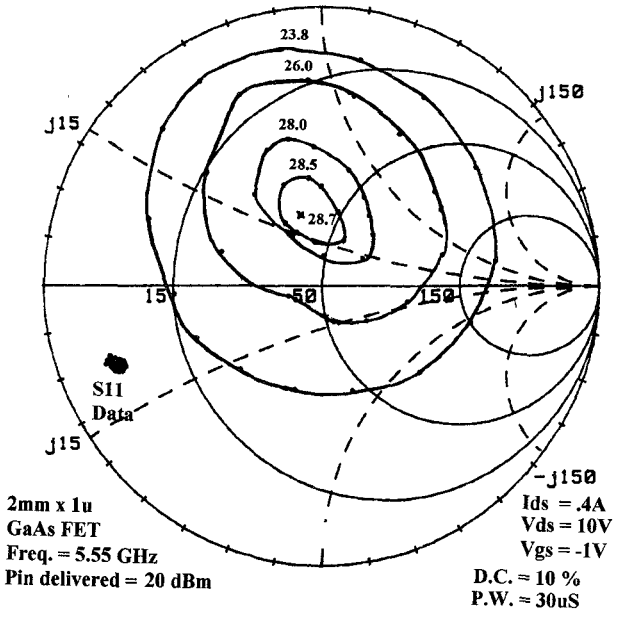



Fig. 7. Measured data for a 2 mm GaAs FET. Data sampled 15 $\mu$S into pulse.

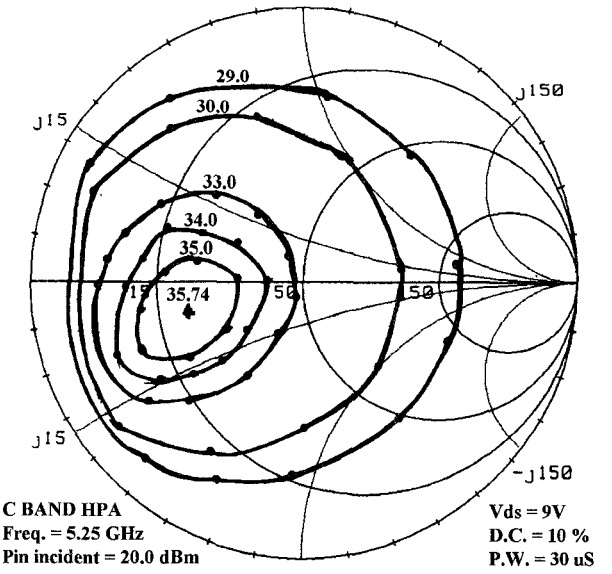



Fig. 8. Measured data for a *C* Band High Power Amplifier MMIC at 5.25 GHz. Data sampled 15 $\mu$S into pulse.

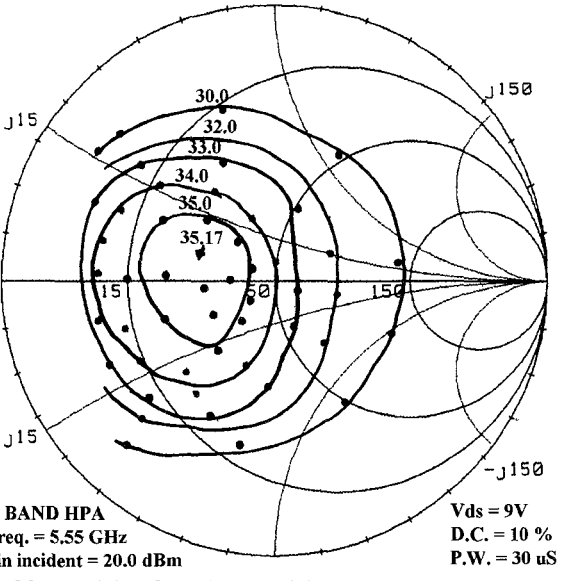



Fig. 9. Measured data for a *C* Band High Power Amplifier MMIC at 5.55 GHz. Data sampled 15 $\mu$S into pulse.

termined from the power incident on the load combined with the measured corrected reflection coefficient of the load. The flow graph for the error correction of the load reflection coefficient is shown in Fig. 6. All the pertinent power levels, the input reflection coefficient, the load reflection coefficient and the forward transmission coefficient are determined from "forward" measurements and one "raw" parameter measurement.

## Measured Results

Several devices were chosen to check out the load pull system. The first verification measurement was a very short thru connection (1 pS). The input reflection coefficient reference plane was extended to be the same as the output "load reflection coefficient" reference plane. It was then verified that both reflection coefficient measurements were identical at all settings of the active load. At the time the data was taken, the contour plotting routines were still in development so the contours were drawn by hand from the recorded data points. Data points were only taken on that part of the load plane that yielded reasonable power output to avoid potential catastrophic damage to the device under test due to severe mismatch.

After operation of the system was verified, a 2 mm wide GaAs FET was selected to be measured on the load pull system. Fig. 7 shows the results taken on one of the 2 mm FET's. The input frequency was chosen to be 5.5 GHz with a delivered input power level of +20 dBm. The drain voltage was set to 10 V and the gate was adjusted for 75% of IDSS. The pulse width was 30 $\mu$S with a 10% duty cycle. The dc and RF data was sampled at 15 $\mu$S into the pulse. The device delivered +28.7 dBm into the optimum impedance. The variation of S11 with load impedance is also shown in Fig. 7.

Another device that was measured on the on-wafer system was a *C* band high power amplifier MMIC. This part was designed to be terminated in a 25 Ω load impedance. The results of the measurements taken at three frequencies are shown in Figs. 8, 9, and 10. The input frequency for Fig. 8 was 5.25 GHz. The input frequency for Fig. 9 was 5.55 GHz. The input frequency for Fig. 10 was 5.85 GHz. The error corrected power incident on the input was +20 dBm. Vds was set at 8 V and the bias was pulsed with a 30 $\mu$S pulse width and a 10% duty cycle. The dc and RF data was sampled at 15 $\mu$S into the pulse. The maximum power delivered for this part was +36.74 dBm into an impedance very close to 25 Ω.

## Future Work

The future work on the on-wafer pulsed active load pull includes completing the contour generation routines, fully automating the measurement and extending the system to

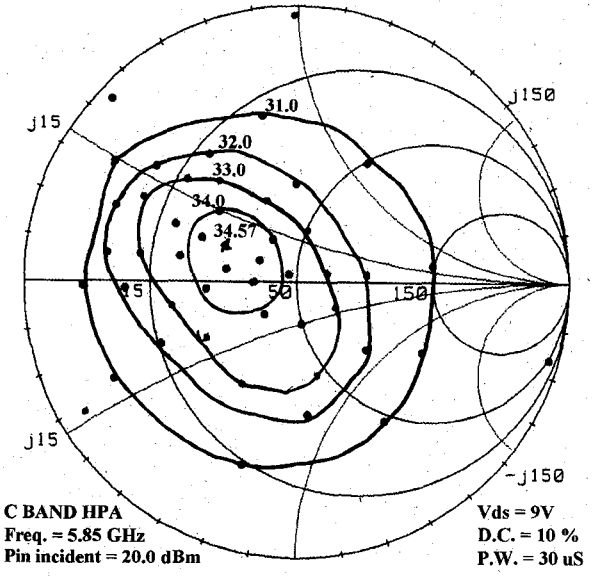



Fig. 10. Measured data for a *C* Band High Power Amplifier MMIC at 5.85 GHz. Data sampled 15 $\mu$S into pulse.

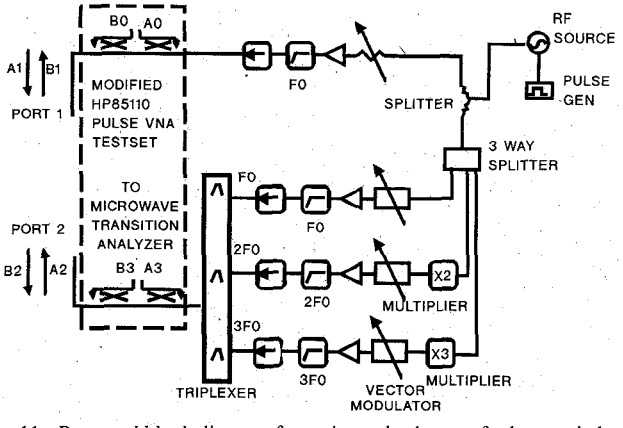



Fig. 11. Proposed block diagram for active pulsed on-wafer harmonic load-pull system.

do on-wafer pulsed active harmonic load pull measurements. At this time, the load pull system software is nearing completion.

The heart of the harmonic load pull effort is the HP71500 microwave transition analyzer. This instrument can make vector measurements of a pulsed signal at the carrier fundamental frequency as well as the first several harmonics up to 40 GHz. It is planned to use this instrument much in the same way as the HP8510B is currently used. The active harmonic load will be configured in a fashion similar to that presented by Larose *et al.* [4]. The proposed block diagram for the pulsed harmonic load pull is shown in Fig. 11. It is currently planned to use the HP8510B as a "error correction" post processor for the HP71500 microwave transition analyzer.

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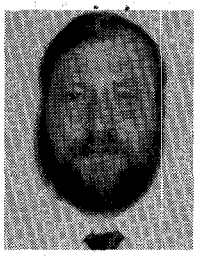

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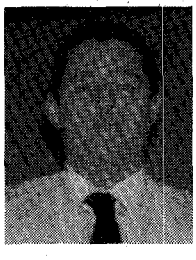

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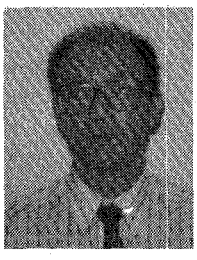
He currently is a MMIC Test Development Staff Engineer for M/A-COM Lowell Semiconductor Operations. He is responsible for development of new test methods to be utilized for on-wafer testing as well as maintenance of the existing on-wafer test systems. He has written the software test manager that is currently in use at M/A-COM LSO and is currently integrating the load pull software into the test manager. He has published several papers involved with on-wafer test techniques.



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